SYSTEM 100

```
                                    ┌──────────────┐
                                    │  NON-RING    │
                                    │   NETWORK    │
                                    │   ELEMENT    │
                                    │     110      │
                                    └──────────────┘
                                            │
                                            │
                                    ┌──────────────┐
                                    │   IN-RING    │
                                    │   NETWORK    │
                                    │   ELEMENT    │
                                    │     102      │
                                    └──────────────┘

┌──────────────┐                                      ┌──────────────┐      ┌──────────────┐
│   IN-RING    │                                      │   IN-RING    │      │  NON-RING    │
│   NETWORK    │        NETWORK RING                  │   NETWORK    │──────│   NETWORK    │
│   ELEMENT    │           114                        │   ELEMENT    │      │   ELEMENT    │
│     108      │                                      │     104      │      │     111      │
└──────────────┘                                      └──────────────┘      └──────────────┘

                                    ┌──────────────┐
                                    │   IN-RING    │
                                    │   NETWORK    │
                                    │   ELEMENT    │
                                    │     106      │
                                    └──────────────┘
                                            │
                                            │
                                    ┌──────────────┐
                                    │  NON-RING    │
                                    │   NETWORK    │
                                    │   ELEMENT    │
                                    │     112      │
                                    └──────────────┘
```

FIG. 1

LINE CARD 202c

PHYSICAL CONNECTION CIRCUITRY 210c

INGRESS PACKET PROCESSING CIRCUITRY 212c

EGRESS PACKET PROCESSING CIRCUITRY 214c

LINE CARD 202d

PHYSICAL CONNECTION CIIRCUITRY 210d

INGRESS PACKET PROCESSING CIRCUITRY 212d

EGRESS PACKET PROCESSING CIRCUITRY 214d

PACKET MESH 226

TDM SWITCHING CIRCUITRY 216

CONTROL CARD(S) 220

LINE CARD 202a

INGRESS PACKET PROCESSING CIRCUITRY 212a

EGRESS PACKET PROCESSING CIRCUITRY 214a

PHYSICAL CONNECTION CIIRCUITRY 210a

LINE CARD 202b

INGRESS PACKET PROCESSING CIRCUITRY 212b

EGRESS PACKET PROCESSING CIRCUITRY 214b

PHYSICAL CONNECTION CIIRCUITRY 210b

NETWORK ELEMENTS 102-108

FIG. 2

MEMORY UNIT 312

| 314a | o o o | 314i |

320 →

FRAMING UNIT 302 ← TRANSMITTING PROTOCOL PROCESSING UNIT 308 ← MEMORY CONTROL UNIT 342 ← EGRESS PACKET PROCESSING CIRCUITRY 214A-D

| 316a | o o o | 316i |

318 →

DEFRAMING UNIT 304 → RECEIVING PROTOCOL PROCESSING UNIT 306 ← MEMORY CONTROL UNIT 340 → INGRESS PACKET PROCESSING CIRCUITRY 212A-D

PHYSICAL CONNECTION CIRCUITRY 210A-D

MEMORY UNIT 310

FIG. 3

MEMORY UNIT 312

408a o o o 408i

TRANSMITTING CHANNELIZING
UNIT 404

314a o o o 314i

320

FRAMING UNIT 302

TRANSMITTING
PROTOCOL
PROCESSING UNIT
308

MEMORY CONTROL
UNIT 342

EGRESS PACKET
PROCESSING
CIRCUITRY 214A-D

316a o o o 316i

318

DEFRAMING UNIT
304

RECEIVING
PROTOCOL
PROCESSING UNIT
306

MEMORY CONTROL
UNIT 340

INGRESS PACKET
PROCESSING
CIRCUITRY 212A-D

406a o o o 406i

RECEIVING CHANNELIZING UNIT 402

MEMORY UNIT 310

PHYSICAL CONNECTION
CIRCUITRY 210A-D

FIG. 4

PORT 510

RESIDUE COUNTER 540

PORT 520

RESIDUE COUNTER 550

PORT 530

RESIDUE COUNTER 560

INTERFACE 570

FIG. 5

610 — TRANSFER DATA ON A FIRST PORT DURING A CURRENT CYCLE UNTIL A PREDETERMINED NUMBER OF BYTES LESS AN OVERSHOOT VALUE HAS BEEN TRANSFERRED ON THE FIRST PORT

620 — CONTINUE TO TRANSFER DATA ON THE FIRST PORT DURING THE CURRENT CYCLE UNTIL A COMPLETE PACKET HAS BEEN TRANSFERRED ON THE FIRST PORT

630 — UPDATE THE OVERSHOOT VALUE FOR THE FIRST PORT BASED ON THE NUMBER OF BYTES TRANSFERRED ON THE FIRST PORT

FIG. 6

FIG. 7

PORT 810

PORT 820

PORT 830

INTERFACE 870

BANDWIDTH
BALANCING
ARBITER
890

INTERFACE 880

PORT 840

PORT 850

PORT 860

FIG. 8

910 SEQUENTIALLY SELECT A PAIR
OF PORTS FROM A PLURALITY
OF PAIRS OF PORTS WHEREIN
THE PAIR OF PORTS COMPRISES
A PORT CONNECTED TO A FIRST
INTERFACE AND A PORT
CONNECTED TO A SECOND
INTERFACE

920 TRANSFER DATA ON THE PORT
CONNECTED TO THE FIRST
INTERFACE DURING A CURRENT
CYCLE

930 TRANSFER DATA ON THE PORT
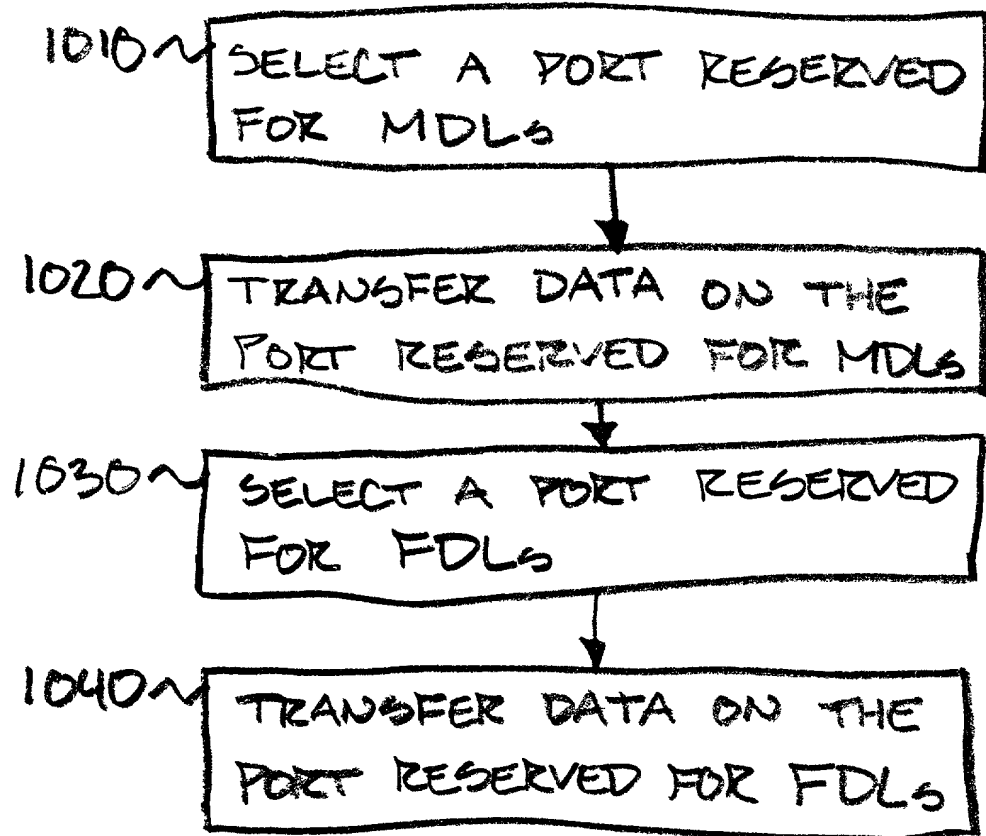CONNECTED TO THE SECOND
INTERFACE DURING THE CURRENT
CYCLE

FIG. 9

1010 ~ SELECT A PORT RESERVED FOR MDLs

1020 ~ TRANSFER DATA ON THE PORT RESERVED FOR MDLs

1030 ~ SELECT A PORT RESERVED FOR FDLs

1040 ~ TRANSFER DATA ON THE PORT RESERVED FOR FDLs

FIG. 10